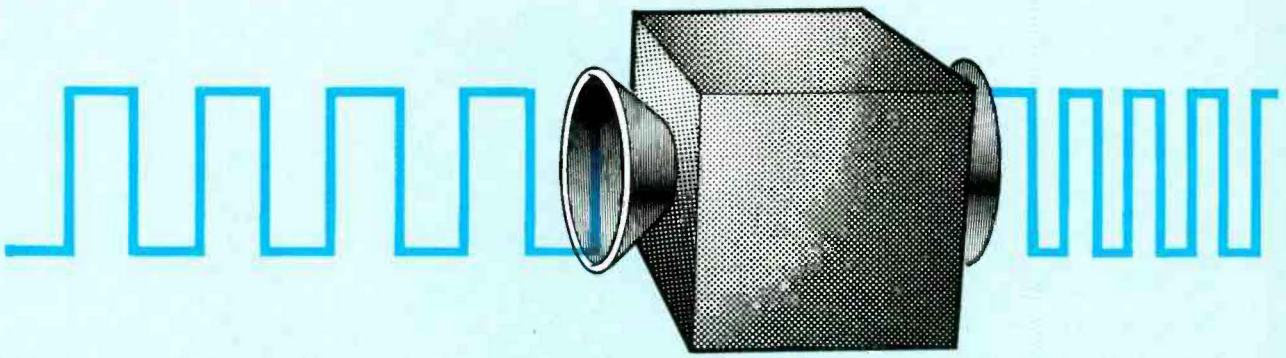

FREQUENCY DOUBLER

Double the frequency of any CMOS or TTL clock signal with this easy-to-build doubler circuit.

JOHN J. YACONO

A UNIVERSAL FREQUENCY-DOUBLING circuit will come in handy in your home shop or on the job. The subject of this article is the construction of a simple circuit that will double the frequency of a digital clock input and be independent of input frequency.

The entire circuit is based on a quad EXCLUSIVE-OR (XOR) gate whose output is 1 (logic high) if any but not more than one of its inputs is 1. The output is 0 if more than one input is 1 or if all inputs are 0. You can make a doubler circuit based on either the CMOS CD4070B or the TTL 74386 because these quad XOR devices are pin-for-pin compatible. A 14-pin socket will permit the devices to be interchanged.

Before discussing construction, some background information on a practical application for the frequency doubler should be helpful, and its theory of operation will be explained.

Consider this situation: You are troubleshooting a digital circuit with a digital logic analyzer and you see that the logic analyzer latches data on the same edge of the clock pulse each time a clock pulse arrives. If you set the analyzer to latch data on the rising edge of a clock pulse, the plot of the clock data will show a constant high. However, if you set the analyzer to latch data on falling transitions, the clock data will appear continuously low. Unfortunately, after you select the desired edge for triggering, you can view only half of the circuit activity and none of the clock transitions.

It is easy to see that under certain circumstances the logic analyzer would be useless. This situation could occur when troubleshooting a microprocessor or microcontroller circuit whose data is latched on one clock transition, processed, and then transmitted on the opposite clock transition.

If you were to view only data collected as it is presented for input or output, it would be impossible to determine if a malfunction were caused by signal-path propagation delays, device propagation delays, settling time, or incorrect processing. Of course, you must distinguish between those three causes to correct them. A digital frequency-doubler that can provide clock pulses for either rising or falling clock pulses (and still remain in-step) would be invaluable.

Operational theory

Propagation delay, a key characteristic of logic gates, is significant in any logic application. It is the time required for a change of logic at the input of a gate to affect the logic at its output. The longer the propagation delays of transistors in a signal path, the longer it takes to produce a usable result. It follows that integrated circuit designers are always trying to minimize propagation delays.

Ironically, a delayed clock signal can be useful in this frequency-doubler circuit. The output of an XOR gate is low when its inputs are equal, and high when its inputs are unequal. Consider what would happen if both a clock pulse and a

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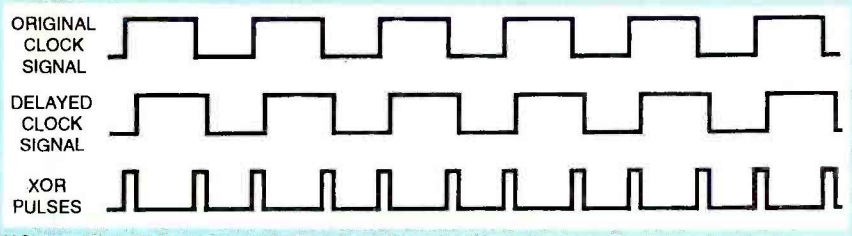

FIG. 1.—IF A PULSE TRAIN (top) is delayed to produce a second pulse train (middle) and both trains are passed into an XOR gate, a pulse train with variable-width pulses will be produced (bottom).

slightly delayed version of the same pulse are applied to the inputs of an XOR gate. The plot of pulses in Fig. 1 shows the original clock pules at the top and a delayed pulse below it.

The output of the XOR gate will appear like the lower waveform in Fig. 1. Thus, the XOR gate generates one pulse for each clock transition. As a result, the gate produces output pulses at twice the clock frequency, but they remain synchronized with the clock, as shown in the upper waveform.

The lower XOR waveform illustrates another important characteristic: the width of the XOR pulses equals the delay introduced to the clock signal or the difference between the rise times of the pules in the top and middle waveforms.

The XOR pulse width will respond to the delay time regardless of frequency with one condition: the delay introduced to the clock signal (the middle waveform) must be shorter than both the high and low times of the clock. Thus, the clock should be delayed by less than 180 electrical degrees if the doubler is to work properly.

This sets the criteria for a circuit that will double clock pulses, but the circuit requires a delayed clock pulse. Because an XOR gate can be configured as a buffer by grounding one of its inputs, and it has an inherent phase delay, the gate will function as delay line to stall clock pulses before they reach a second XOR gate.

The circuit

The frequency doubler circuit is shown in Fig. 2. It is powered by the DUT. This eliminates the need for additional circuitry and also "configures" the doubler to operate at appropriate logic-voltage levels. This is necessary for testing CMOS logic because of the wide range of operating voltages and logic levels.

In Fig. 2, IC1-a is the pulse-producing gate, and IC1-b, IC-c, and IC1-d form a variable-delay network. Each gate in the network adds its phase delay to the signal it receives. Thus, IC1-b delays the clock by one phase delay period, IC1-c delays it for an equal period, and IC1-d adds yet another delay.

The gates are arranged so that both the phase delay and the width of the output pulses can be selected by making wire changes on a header that carries the delayed signal to IC1-a. That feature has two functions: 1) it extends the duration of the output pulses for slower test equipment, and 2) decreases the pulse width for testing very fast circuits.

As stated earlier, you have a choice of quad XOR IC: a CMOS CD4070B or equivalent in a faster CMOS family (HC/HCT, HCS/HCTS, or ACL (FACT)) or a 74386 or its equivalent in faster TTL logic families (AS, LS, ALS, FAST). Your selection will determine the propagation delay of the gates. The delay is important because it determines the maximum input frequency that the circuit can handle and the maximum pulse width it can generate.

Maximum input frequency will limit the circuitry with which the doubler will be effective. Maximum pulse width will permit the circuit to work with the slowest test equipment. (Additional gates can be added to the delay network to increase the output pulse width for the slowest equipment.) To maximize the doubler's versatility, select a quad XOR with the highest maximum frequency that is compatible with your test equipment.

Table 1 provides information to help you select the optimum TTL family for your needs. The propagation delays are typical values obtained from data books, but devices from different manufacturers might have different typical values. The maximum output pulse widths given in the table were obtained by multiplying the

TABLE 1—TTL PROPATATION DELAYS VS. DOUBLER FREQUENCY LIMITS

TTL Family	Typical Delay (ns)	Maxcimum Input Frequency (Hz)	Longest Output Pulse (ns)
Advanced Schottky	1.5	166,667	4.5
Fast Schottky	2	125,000	6
Schottky	3	83,333	9
Advanced Low-power TTL	6	41,667	18
Low-Power Schottky	9	27,778	27
Standard TTL	10	25,000	30
Low-Power TTL	33	7,576	99

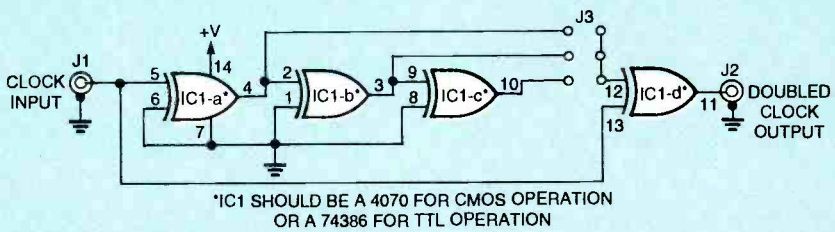

FIG. 2.—THE ACTIVE COMPONENT OF THE FREQUENCY DOUBLER is a quad exclusive-or (XOR) gate.

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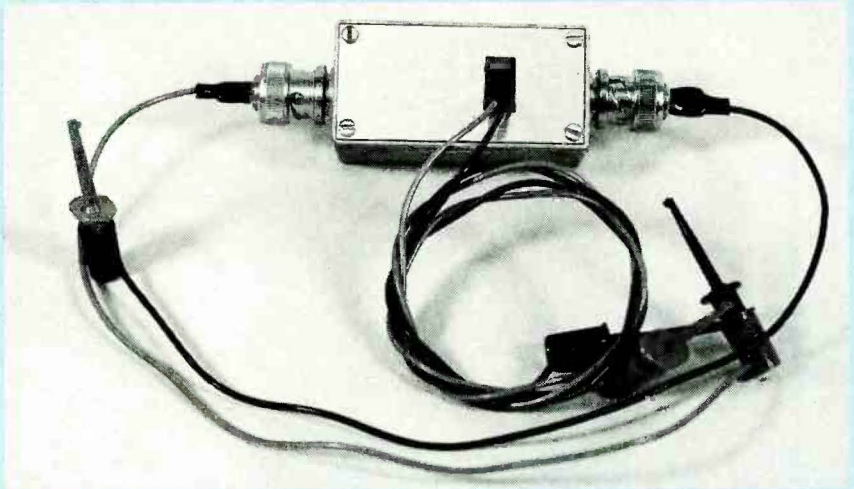
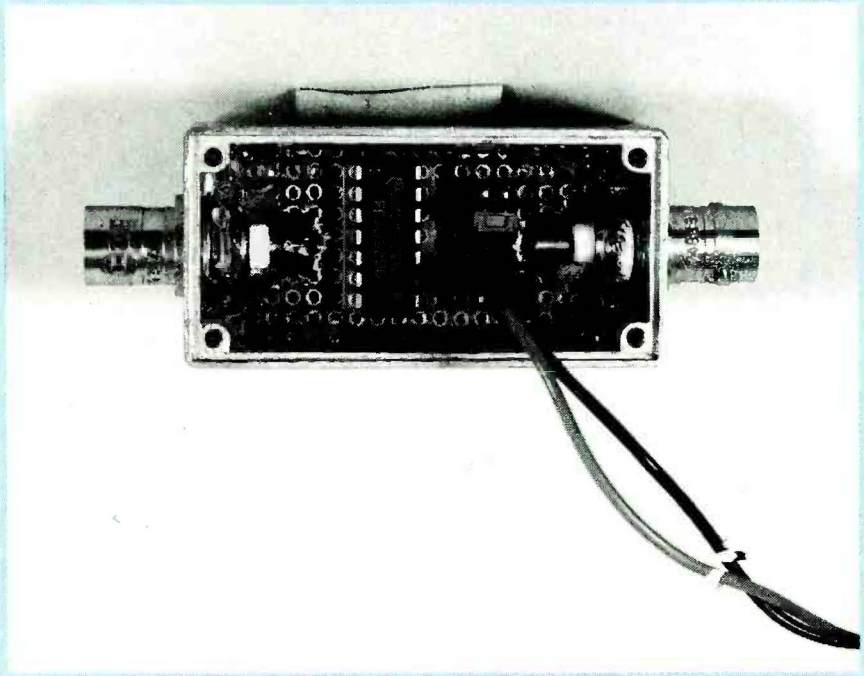


FIG. 3—COMPLETED FREQUENCY DOUBLER. The power leads are fitted with microclips and attached to two extra pins on the jumper block.



A JUMPER BLOCK was substituted for a triple-throw switch to conserve space.

propagation delay by a factor of 3 (the number of delay gates in the delay network).

Deciding on a CMOS IC is easier because even the fastest CMOS ICs are slower than the response times in most test equipment. A device from the high-speed HCT CMOS family is suitable for testing CMOS circuits that are powered by 5 volts, but a standard 4000B series IC will be suitable for testing all other CMOS circuits.

PARTS LIST

Semiconductor

IC1—quad XOR-gate, CMOS or TTL (see text)

Other components

J1, J2—BNC jacks, wall mount

J3 (S1)—four-pin header, PCB mount (or triple-throw switch, see text)

Miscellaneous: Project case (metal, see text), two BNC plugs, two microclips, 14-pin IC socket (see text), perforated construction board, heat-shrink tubing, insulated hookup wire, solder.

Doubler construction

The doubler circuit's 14-pin IC is mounted in a 14-pin DIP socket on a rectangular piece of perforated construction board. (Regardless of assembly method—wire wrapping or point-to-point wiring—keep all wires as short as possible.) If you design your own PC board, design in a ground plane on the reverse side.

Select a metal project case with a metal cover that will provide good shielding. The prototype is housed in an aluminum case measuring 5¼ × 3 × 2⅛inches. Holes are drilled in both ends of the metal case for BNC jacks J1 and J2. Another hole is cut in the case cover to allow the power and ground wires to exit.

In order to fit the circuit in such a small case, a 4 × 2 shorting header was used in place of a triple-throw switch for S1. The S1 connections are then made by moving a jumper. The two extra pins on the shorting jumper have leads attached to them for obtaining power and ground from the DUT. (You can prevent shorting between the closely-spaced power and ground jumper header pins with heat-shrinkable tubing, if necessary.) If you can find a small triple-throw switch you can use that, or use the header instead (as we did) or use a larger switch and bigger case.

Position the completed circuit board in the bottom of the case and fasten it in place with double-sided tape or RTV silicone. Pass the power leads through the hole in the cover and terminate them with microclips. Figure 3 shows the assembled frequency doubler ready to be put to work.

Testing the doubler

To test out the frequency doubler, feed in a signal of known frequency from a crystal-based reference or function generator and measure the output frequency with a frequency counter or oscilloscope. The doubler will double the input frequency if it is functioning correctly.

The details will not be described in this article, but you can increase the versatility of the frequency doubler by fitting it with an analog front end. An operational amplifier configured as a Schmitt trigger will perform this function. Ω

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